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| 10/524,981 | 02/18/2005 | Paul Van Der Sluis | NL03 0866 US | 3943 |

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| EXAMINER | |
|---|---|
| BUDD, PAUL A | |
| **ART UNIT** | **PAPER NUMBER** |
| 2815 | |

| SHORTENED STATUTORY PERIOD OF RESPONSE | MAIL DATE | DELIVERY MODE |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/524,981 | VAN DER SLUIS ET AL. | |
| | Examiner | Art Unit | |
| | Paul A. Budd | 2815 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *05 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) *1-15 and 24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *16-20, and 22-23* is/are rejected.

7)☒ Claim(s) *21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/18/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

1. Applicant's election without traverse of Group II claims **16-23** in the reply filed on 5 April 2007 is acknowledged. The amendments to the claims are accepted and no new matter is entered. Also claims **1-15** and **23** are withdrawn without prejudice. The Office believes the applicant made a typographical error in including claim **24** with the current election since claim **24** recited a method. However, the method of operating the device was grouped into Group I not Group II. The Office will proceed without examination of unelected claim **24** based on this understanding.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim **20** recites the limitation "and the source or drain region of the field effect transistor" in lines 4-5. There is insufficient antecedent basis for this limitation in the claim. For the purposes of examination it will be assumed that claim **20** is dependent on claim **19** and not claim **17** since there is no mention of a source or drain or field effect transistor in claims **16-17**. Claim **19** appears to be the most logical choice.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims **16-18,** and **22** rejected under 35 U.S.C. 102(b) as anticipated by Nakao et al. (US Pat 5,303,182).

Regarding claims **16** Nakao teaches a method of manufacturing a ferroelectric device wherein a body is formed that comprises a substrate [FIG.5, 11], and

the device is provided with a ferroelectric layer [FIG. 5, 16] having a connection conductor [FIG. 5, 17; column 5, lines 23-67 to column 6, lines 1-48] on a side facing away [see FIG. 5] from the substrate [11],

an oxygen-free ferroelectric material [column 5 lines 34-38] being selected as the material for the ferroelectric layer [FIG. 5, 16] which is used to form an active electrical element, characterized in that a conductive layer [FIG. 5, 15] is provided between the substrate [11] and the ferroelectric layer [16],

which conductive layer [15] forms a further connection conductor [15] of the ferroelectric layer [16], and

the memory element is obtained by forming a Schottky junction [column 6, 18-20] between the ferroelectric layer [16] and at least one of the connection conductors [15].

Additionally, a Schottky junction is formed according to the applicant's specification by use of the applicant's material teachings i.e.; platinum (applicant page 8, lines 7-9) as the "further connection conductor" (Nakao, column 6, lines 18-19, "platinum") and an oxygen free ferroelectric material (page 1 lines 20-29 to page 2 lines 1-8, and page 8 line 23 to page10 line 33) {Nakao "$BaMgF_4$, $NaCaF_3$... $Zn_{1-x}Cd_xTe$" column 5 lines 35-38}.

Regarding claim **17** Nakao teaches a method according to claim **16**, characterized in that the active electrical element is formed as a memory element [column 6, line 28 to column 8 line 48].

Regarding claims **18** Nakao teaches a method as claimed in claim **17**, characterized in that the body is formed so as to be a semiconductor body [FIG. 5-7(a), 11 or 101], and a semiconductor substrate [column 5, lines 8-18; FIG. 5-7(a), 11 or 101] is selected as the substrate [11 or 101].

Regarding claims **22** Nakao teaches a method as claimed in claim **17**, characterized in that a matrix of N x M memory elements is formed [FIG. 8, column 6 line 67 to column 10 line 22], where N and M are natural numbers and each memory element is provided on both sides with an electric connection [FIG. 8 teaches the memory element provided on both sides with an electrical connection].

4. Claims **16-20,** and **22-23** rejected under 35 U.S.C. 102(b) as anticipated by Itoh et al. (US Pat 5,965,942) or, in the alternative, under 35 U.S.C. 103(a) as obvious over Itoh et al. (US Pat 5,965,942).

Regarding claims **16** Itoh teaches a method of manufacturing a ferroelectric device
wherein a body is formed that comprises a substrate [FIG. 1, 1], and
the device is provided with a ferroelectric layer [FIG. 1, 9] having a connection conductor [10] on a side facing away from the substrate [1],
an oxygen-free ferroelectric material [column 6, line 2, $BaMgF_4$] being selected as the material for the ferroelectric layer [9] which is used to form an active electrical element,
characterized in that a conductive layer [FIG. 1, 7,8] is provided between the substrate [1] and the ferroelectric layer [9],
which conductive layer [7,8] forms a further connection conductor [7,8] of the ferroelectric layer [9], and
the memory element [FIG. 1] is obtained by forming a Schottky junction between the ferroelectric layer [9] and at least one of the connection conductors [7,8, column 6, lines 5-10].
A Schottky junction is formed according to the applicant's specification by use of the applicant's material teachings i.e., platinum (applicant page 8, lines 7-9) as the "further connection conductor" (Itoh, column 6, lines 5-10, "platinum") and an oxygen free

ferroelectric material (page 1 lines 20-29 to page 2 lines 1-8, and page 8 line 23 to page10 line 33) {Itoh "$BaMgF_4$" column 6 line 2}.

Regarding claims **17** Itoh teaches a method according to claim **16**, characterized in that the active electrical element [FIG. 1] is formed as a memory element [column 1-2].

Regarding claims **18** Itoh teaches a method as claimed in claim **17**, characterized in that the body is formed so as to be a semiconductor body [FIG. 1, 1], and a semiconductor substrate [column 3, lines 15-20] is selected as the substrate [1].

Regarding claims **19** Itoh teaches a method as claimed in claim **17**, characterized in that in the semiconductor body there is formed a field effect transistor [FIG, 1; 4,3,4; column 3, lines 19-21 and 46-48] with a source region [4], a drain region [4] and a gate electrode [3], and the further connection conductor [7,8] is provided on the source [4] or drain region [4] of the field effect transistor [4, 3, 4] and is formed so as to be a connection conductor [7,8] of the source region [4] or drain region [4].
There is nothing in claim **19**'s limitations that forbids or excludes the existence of a polysilicon plug between the source [4] and the connection conductor [7,8].

Regarding claims **20** Itoh teaches a method as claimed in claim ***19***, characterized in that the Schottky junction is formed [as explained above for claim **16**] between the further connection conductor [7, 8] and the ferroelectric layer [9], and an ohmic contact [Table

1, column 5] is formed between the connection conductor and the ferroelectric layer as well as between the further connection conductor and the source or drain region of the field effect transistor [by means of the polysilicon plug].

As for claims **22** and **23** Itoh teaches the method as claimed in claim **17** but does not explicitly state forming a matrix of N x M memory elements with each memory element is coupled to a field effect transistor with N first conductor tracks, M second conductor tracks etc. However these connections are array configuration are well known in the art for memories and are considered obvious uses of a memory cell,

### *Allowable Subject Matter*

5. Claim **21** objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### *Conclusion*

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Wolf et al. (US Patent 5,512,773) and Lampe et al. (5,146,299).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul A. Budd whose telephone number 571-272-8796. The examiner can normally be reached on Monday to Friday 8:30 to 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PAB

JEROME JACKSON
PRIMARY EXAMINER